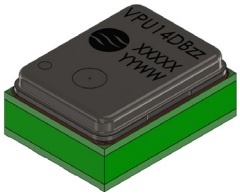
Description



The Sonion Voice Pick Up (VPU) Sensor is a high-performance bone conduction sensor optimized for picking up a user’s own voice. The VPU Sensor enhances communication in noisy/challenging types of environments. Picking up your own voice via vibrating bones in your skull, results in an intelligible voice with high SNR and without the ambient sound/background noise. This highly intelligible signal from the VPU is perfect for accurately controlling a voice operated input system. This signal can also be used for anti-occlusion purposes.

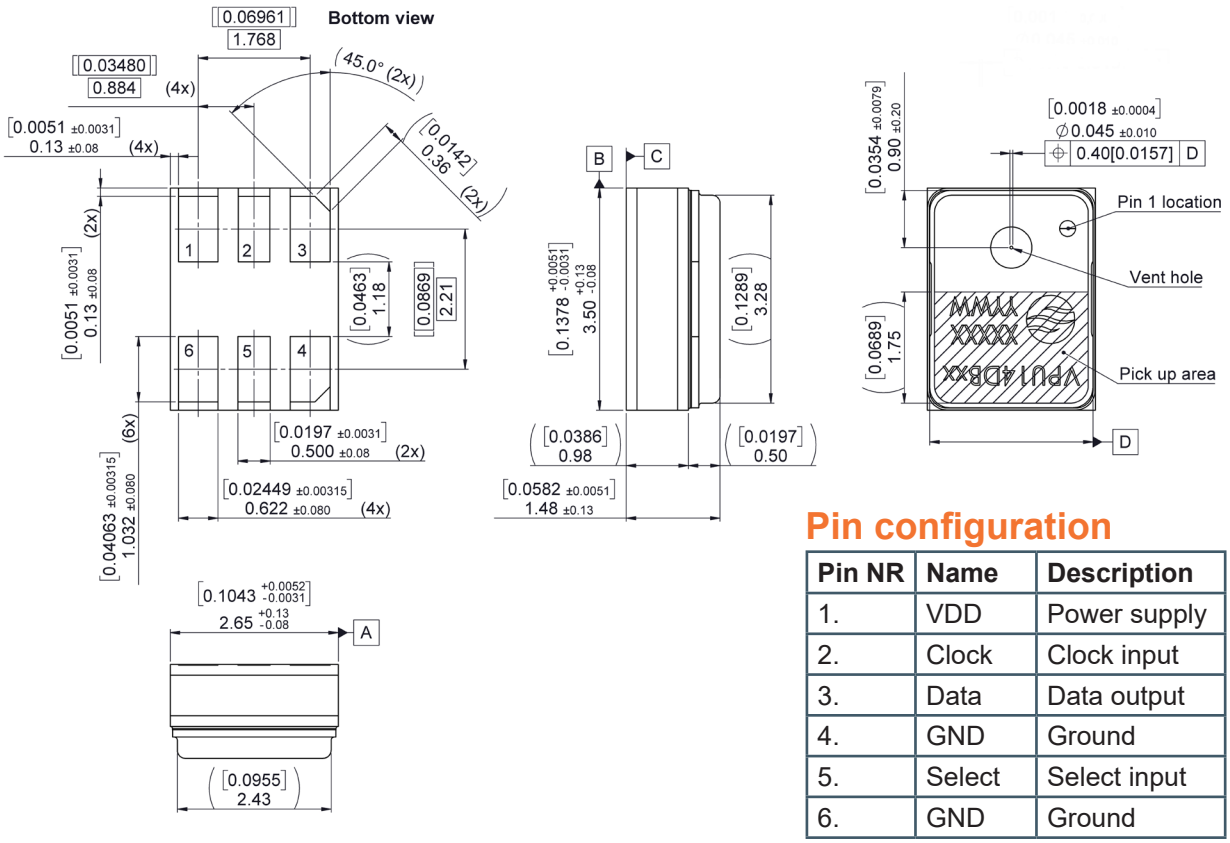
Applications

- Hearable / wearable devices, such as True Wireless Stereo earbuds, smart glasses, head worn devices, intelligent glasses, VR glasses
- On- / Over-ear headphones
- Professional headsets, such as call center headset, pilot headset, motorcycle headset
- Communication systems
- Smartphones

Features

- Small size 3.5 x 2.65 x 1.50 (13.9 mm^3)
- Digital pulse density modulation (PDM) output interface
- High bone conduction sensitivity (-12 dBFS/g) with ultra-low noise (-75.5 dBg)
- Large bandwidth up to 8 kHz
- Optimized for picking up users’ own voice on different positions of human head
- Ultra-low power consumption (typ 120 µA), designed to help save battery life in continuous active mode
- Zero halogens
- REACH & RoHS compliant
- Reflow solderable (SMD)
- Full hermetic package in application

Product drawing - Dimensions in mm



Pin configuration

Pin NR	Name	Description
1.	VDD	Power supply
2.	Clock	Clock input
3.	Data	Data output
4.	GND	Ground
5.	Select	Select input
6.	GND	Ground

Specifications (normal mode)

All parameters are specified with closed vent at 1.8 V supply voltage, f(clock) 768 kHz, 32x decimation ratio and with ~70pF load impedance unless specified otherwise.
Environmental conditions: 23°C (73.4F), 50% RH.

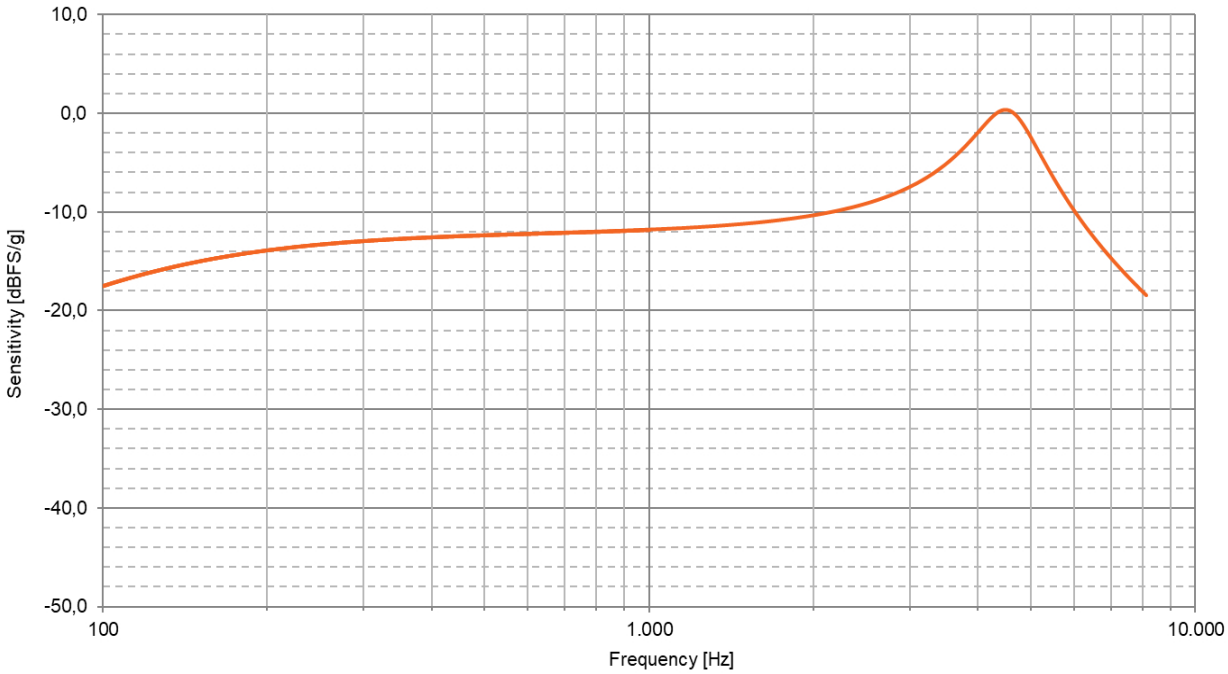
Performance		Min	Typ	Max	Unit	Comments
Sensitivity	@ 130 Hz	-6	-3	0	dB	re. 1 kHz value
	@ 1 kHz	-15	-12	-9	dBFS	re. 1g
Resonant peak	frequency	4	4.5	5	kHz	
	amplitude	9	12	15	dB	re. 1 kHz value
EIN (A-weighted)	100 Hz-8 kHz		-75.5		dBg	
Noise floor	100 Hz-8 kHz		-88		dBFS	
1/3 Octave equiva-lent input noise	@ 250 Hz		-87		dBg	
	@ 1 kHz		-88.5		dBg	
	@ 2 kHz		-89		dBg	
Noise density	@ 250 Hz		6		µg/√Hz	
	@ 1 kHz		2.5		µg/√Hz	
	@ 2 kHz		1.7		µg/√Hz	
Max input level			3.5		g	for typ THD <10% @ 1 kHz
			0.8		g	for typ THD <10% @ 4.5 kHz

Electrical	Min	Typ	Max	Unit	Comments
Supply voltage (V_{DD})	1.62	1.8	3.6	V	
Supply current	85	120	155	µA	no load
Power supply rejection ratio (PSRR)		54		dBFS/V	200m Vpp, 1 kHz, sine wave
Power supply rejection (PSR)		-80		dBFS	100m Vpp, 217 Hz, square wave, A-weighted

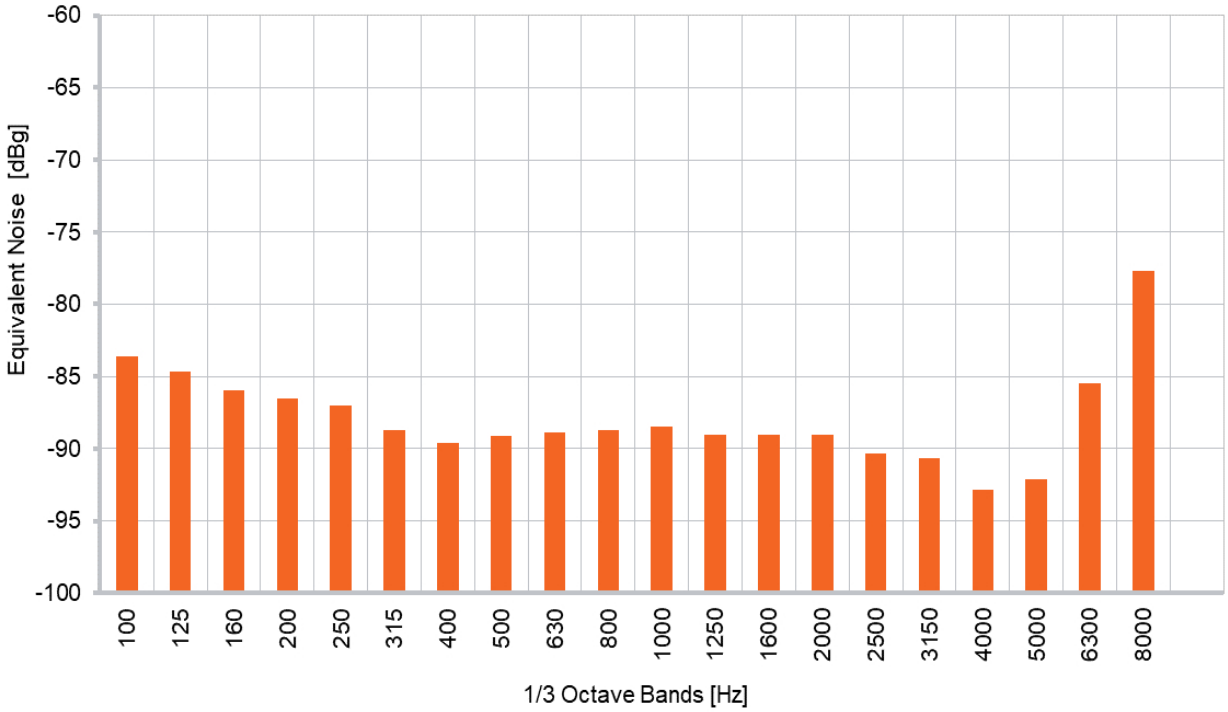
Absolute Maximum Rating

Parameters	Min	Typ	Max	Unit	Comments
Shock resistance			10k	g	tested with 50 grams fixture in all 3 directions
Operating temperature	-40		85	°C	
Storage temperature	-40		105	°C	

Typical sensitivity characteristic



Typical 1/3 octave equivalent noise



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NL: +31 20 6068 100

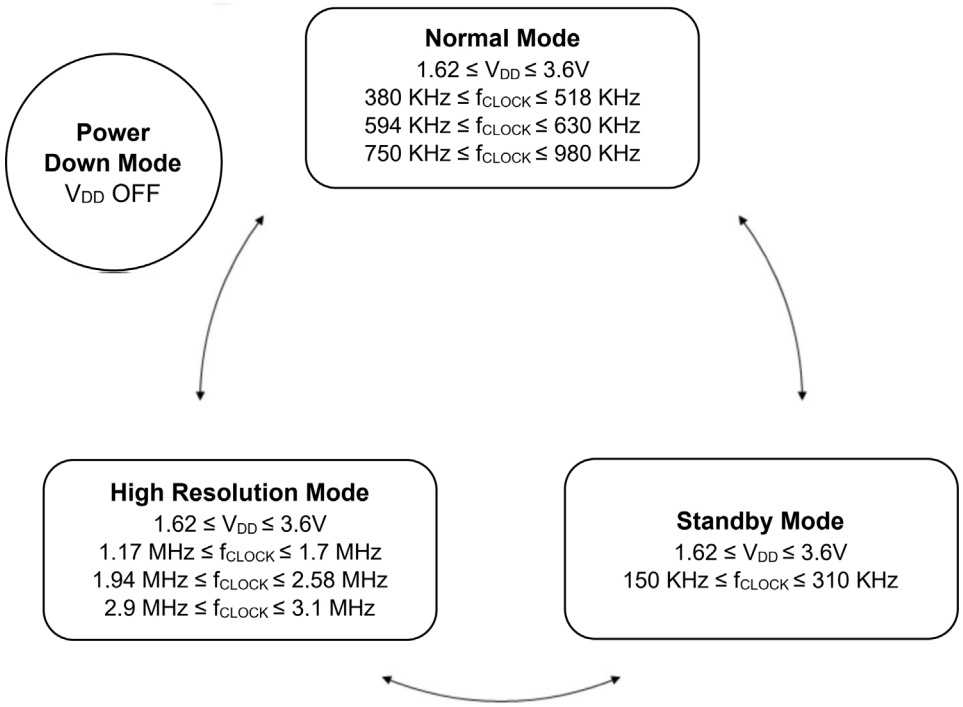
Electrical specifications

Environmental conditions: 25±2°C (77±3.6 F), 60±10% RH.

Items	Symbol	Condition	Limits			Unit
			Min	Nom	Max	
Data format		1/2 cycle PDM				
Clock duty cycle			40		50	%
			45		55	%
Clock frequency	f_{clock}	High resolution operation	1.94	2.4	2.58	MHz
		Normal operation	750	768	980	kHz
		Standby mode	150		310	kHz
Clock off mode current	I_{clock_OFF}	Clock pulled low.		<1	10	µA
Standby mode current	$I_{standby}$				50	µA
Clock rise/fall time	t_{edge}				13	ns
Logic input low	V_{IL}	I_{out} = 0.5 mA	-0.3		0.35xV_{DD}	V
Logic input high	V_{IH}	I_{out} = 0.5 mA	0.65xV_{DD}		V_{DD}+0.3	V
Logic output low	V_{OL}	I_{out} = 0.5 mA			0.3xV_{DD}	V
Logic output high	V_{OH}	I_{out} = 0.5 mA	0.7xV_{DD}			V
Delay time for data valid	t_{valid}	Delay time for clock edge (50%V_{DD}) to data valid. (<0.3xV_{DD} or >0.7xV_{DD})			100	ns
Delay time for high Z	t_{HZ}	Delay time for clock edge (50%V_{DD}) to data high impedance state	5		30	ns
Delay time for data driven	t_{DD}	Delay time for clock edge (50%V_{DD}) to data driven	40		80	ns

Note: Electrical parameters are guaranteed by MEMS/ASIC design.

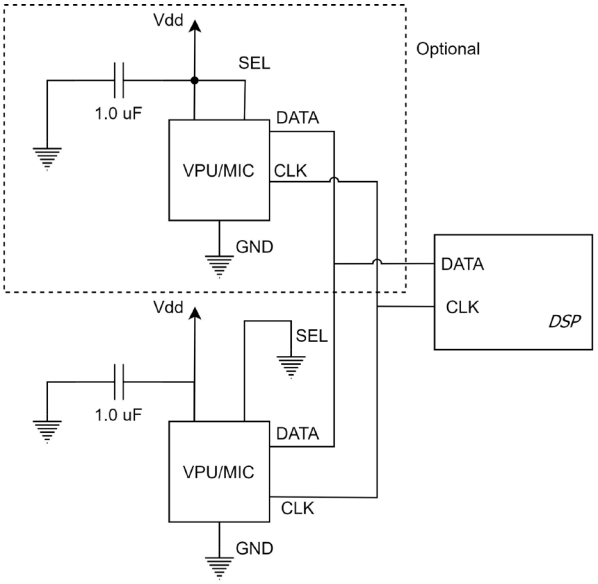
VPU State Diagram



Mode	Clock frequency		Current	
	Typ.	Unit	Typ.	Unit
Normal mode	480	kHz	110	µA
	600	kHz	120	µA
	768*	kHz	120	µA
High resolution mode	1.536	MHz	350	µA
	2.4	MHz	490	µA
	3.072	MHz	560	µA
Standby mode			<50	µA

* Default clock frequency

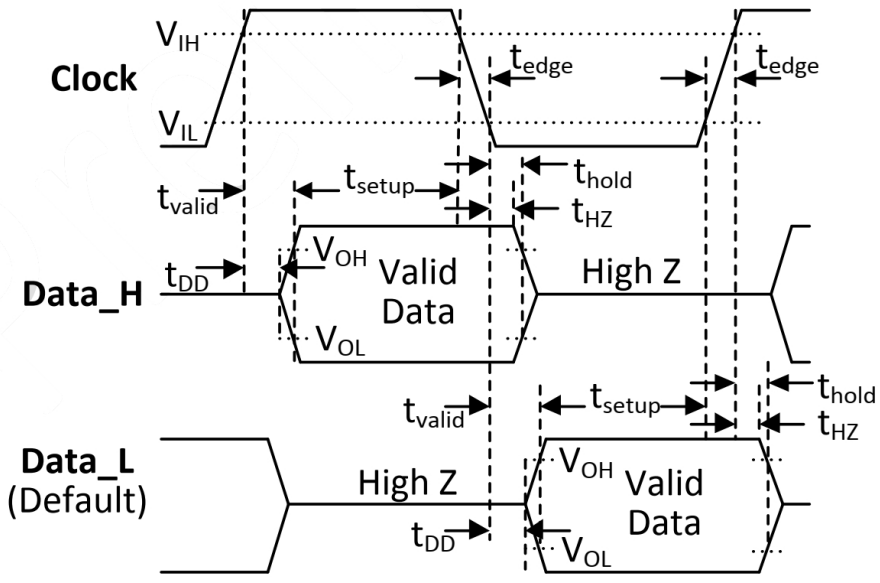
Recommended interface circuit



A 1µF bypass capacitor shall be placed close to the VPU VDD pad to ensure the best SNR.

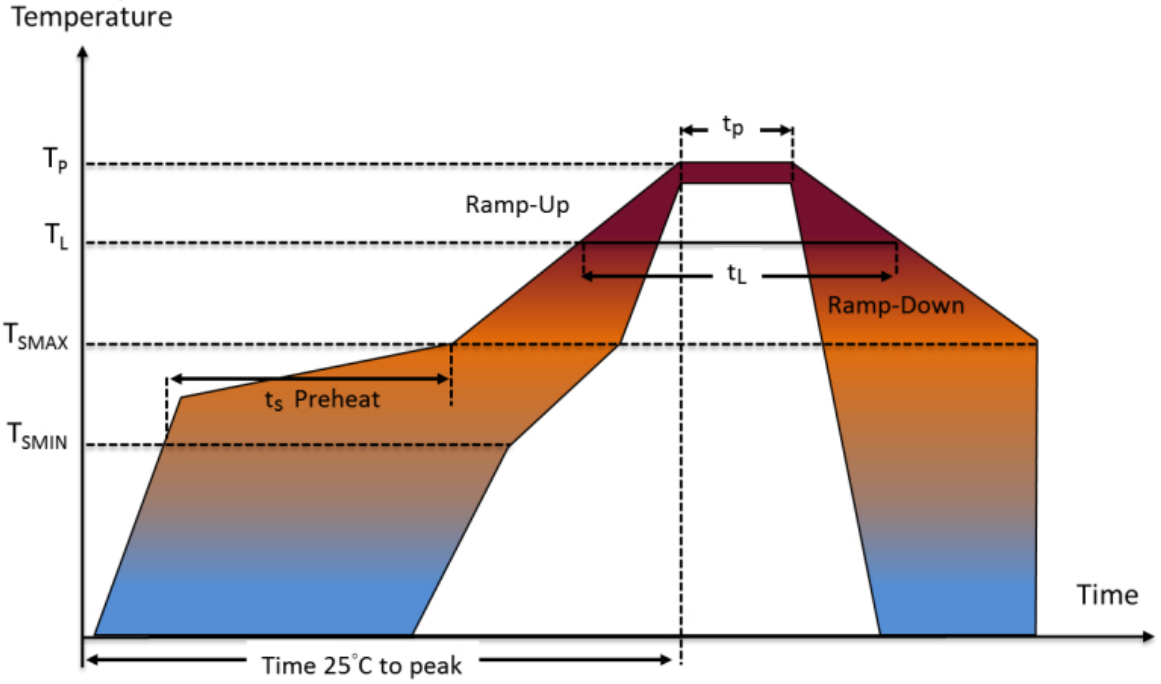
Label	Select	Drives Data After	High-Z After
Data_H	High	Rising Clock Edge	Falling Clock Edge
Data_L	Low (default)	Falling Clock Edge	Rising Clock Edge

Timing diagram



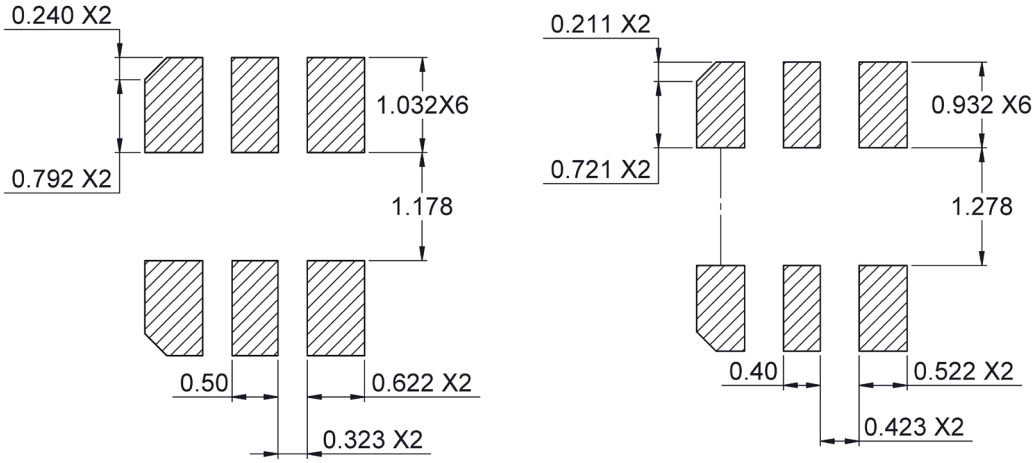
$$T_{clock}/2 = t_{edge} + t_{valid} + t_{setup}$$

Soldering profile



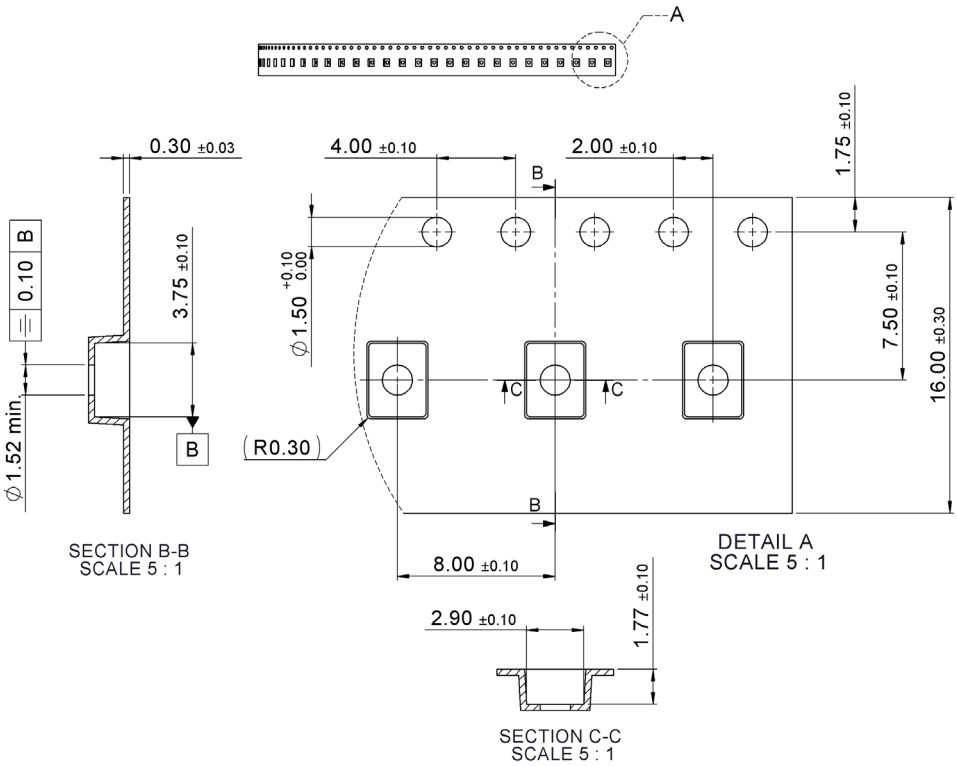
Profile feature	Temperature profile (T)	Time (t)
Preheat (ts) (T_{SMIN} to T_{SMAX})	T_{SMIN} = 150°C T_{SMAX} = 180°C	60-100 seconds
Peak temperature (T_P) Time within 5°C of actual peak temperature (t_P)	T_P = 260°C (max)	20-30 seconds
Time maintained above liquidus (T_L)	T_L = 220°C	40-80 seconds
Ramp-up (T_{SMAX} to T_L)	180°C to 220°C	1.25°C/second max
Ramp-down (T_P to T_{SMAX})	245°C to 220°C	3°C/second max
Time 25°C to peak temperature	---	8 minutes max
No failure with 3x reflow		

Recommended PCB land pattern layout (left) and recommended solder paste stencil pattern layout (right). Scales are in mm.



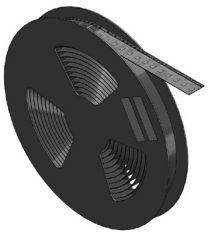
Packaging - Dimensions in mm

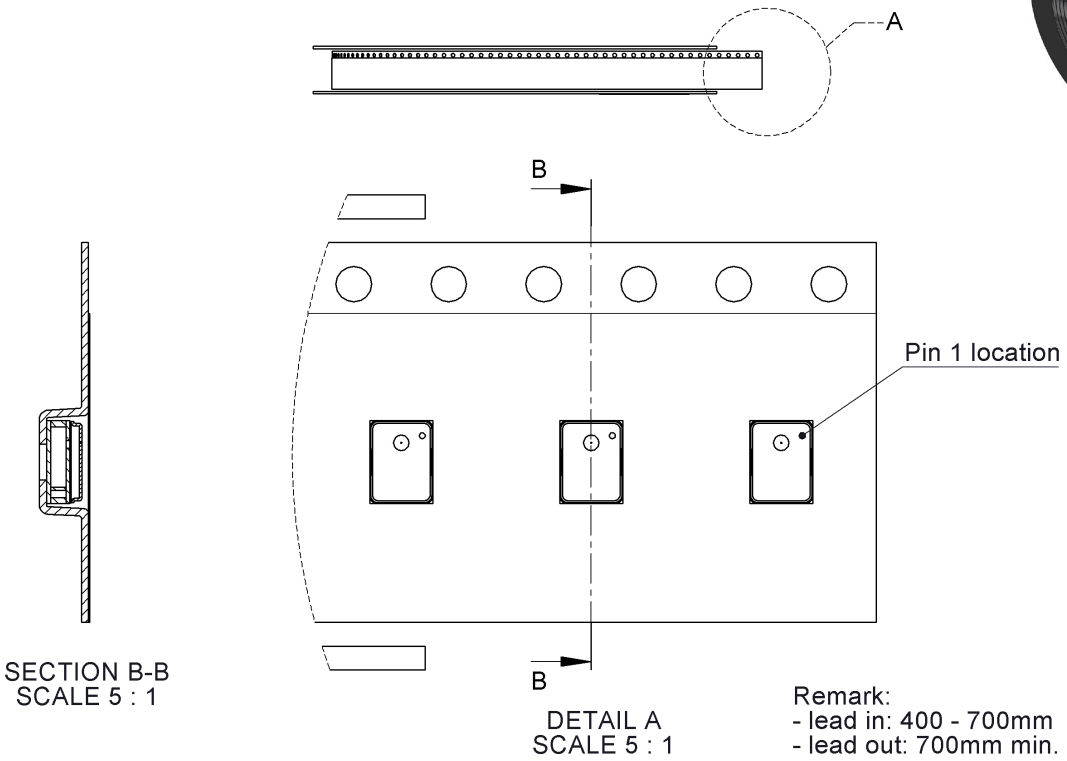
Reel diameter 180 mm (7 inch)



Packaging - Product orientation

Maximum quantity per reel 1000





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